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Optimal Bus Capacitance Design for System Stability in On-Board Distributed Power Architecture

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Abstract— Recently, the distributed power system is mainly used for the power supply system which requires the low-voltage / high-current output. The distributed power system consists of bus converter and POL. The most important factor is the system stability in bus architecture design. The overlap between the output impedance of bus converter and input impedance of POL causes system instability, and it has been an actual problem. Increasing the bus capacitor, system stability can be reduced easily. However, due to the limited space on the system board, increasing of bus capacitors is impractical. The urgent solution of the issue is desired strongly. This paper presents the output impedance design for on-board distributed power system by means of three control schemes of bus converter. The output impedance peak of the bus converter and the input impedance of the POL are analyzed, and it is conformed by experimentally for stability criterion. Furthermore, the optimal intermediate bus capacitance design for system stability is proposed.

Keywords— Distributed power system, bus converter design, output impedance, intermediate bus capacitance.

I. INTRODUCTION

Various LSI is used in the telecommunication application equipments and the driving voltage is various. On the other hand, increase of load current is also remarkable by advanced function of LSI. Since the present LSI is designed in accordance with semiconductor manufacture technology, the tolerance level of operation voltage is very narrow. Consequently, the voltage drop by the wiring impedance of power line causes malfunction of LSI. In order to reduce the malfunction of LSI by the voltage drop, it is proposed that the converter is arranging very close to the LSI. This converter is called POL. Thus, the power supply system which requires the low-voltage / high-current output has been changing from conventional centralized power system to distributed power system. The distributed power system consists of first-stage isolated DC-DC converter as a bus converter and second-stage non-isolated DC-DC converter as a POL. However, the instability phenomenon in a distributed power system is posing a problem recently. This is instability phenomenon resulting from overlapping between the output impedance of bus converter and the input impedance of POL. Increasing the bus capacitor, system stability can be reduced easily. However, due to the limited space on the system board, increasing of bus capacitors is impractical. The urgent solution of the issue is desired strongly, and the various discussion of system stability has been reported[1-8]. Then, we also have reported the detailed discussion of system stability by control schemes of bus converter (Un-regulated, Semi-regulated and Full-regulated)[9-14]. However, so far, the detailed discussion of practical design and the optimal intermediate bus capacitance design of bus converter about on-board distributed power system has not been reported. This paper presents the optimal design of bus converter for on-board distributed power system by means of three control schemes of bus converter.

II. DISCRIMINATION OF STABILITY

Figure 1 shows the distributed power system consisting of bus converter and POL. Even if each converter has stable operation, the instability phenomenon may occur by connecting two converters in series. Bus converter and POL have input-to-output voltage transfer function Gvb(s) and Gvp(s), respectively. The overall input-to-output voltage transfer function Gvv(s) is given following equation;

\[ G_{vv}(s) = \frac{G_{vb}(s)G_{vp}(s)}{1 + Z_o(s)/Z_in(s)} \]  

where Zo(s) is the output impedance of bus converter, and Zin(s) is the input impedance of POL. From Eq. (1), the input and output impedance is greatly concerned with the system stability. The stability of closed-loop system is decided with the characteristics equation 1+Zo(s)/Zin(s). This means relation between Zo(s) and Zin(s) decides the system stability. This system may become unstable when both impedances are overlapped, as shown in Fig. 2 (a). It is necessary to eliminate this impedance overlap for system stability. However, eliminating this impedance overlap for all frequency range is very difficult.

![Fig. 1. On-board distributed power system.](image)
On the other hand, it may have stable operation even if both impedances are overlapped. This is because the phase margin becomes large under the influence of the input impedance. When the bandwidth of POL is enough wider than the bandwidth of bus converter, if the peak value of output impedance becomes almost equal to the steady-state value of input impedance \( |Z_{in}(0)| \) as shown in Fig. 2 (b), then this system becomes stability limit as shown in Fig. 2 (b). Moreover, this system becomes unstable if the peak value of output impedance exceeds \( |Z_{in}(0)| \). From mentioned above consideration, the new stability criterion can be defined as follows[15].

\[
\begin{align*}
|Z_{in}(0)| \geq Z_{o,\text{peak}} & : \text{Stable} \\
|Z_{in}(0)| < Z_{o,\text{peak}} & : \text{Unstable}
\end{align*}
\]

### III. IMPEDANCE ANALYSIS

The half-bridge converter with the most popular circuit of the power-stage is used as a bus converter, and the synchronous buck converter with the most popular circuit is used as POL. Figure 3 and 4 show the circuit diagrams, respectively. The output impedance of bus converter and the input impedance of POL can be derived by applying the stage space averaging method[16,17].

#### A. Input Impedance

At first, the low-frequency value \( |Z_{in}(0)| \) of input impedance is estimated. The input impedance of POL can be derived as following equation[18].

\[
Z_{in}(s) = \frac{s^2 L_b C_b r_{in}}{s^2 L_b C_b + sC_b (r_{in} + r_{o}) + 1}
\]

where,

\[
T_b(s) = k \cdot \text{PWM} \cdot G_{dv} (s)
\]

\[
G_{dv} (s) = \frac{V_s}{P(s)} (sC_r + 1) \quad (V_s = V_{in}/2n)
\]

\[
P_i(s) = s^2 L_b C_b + sC_b (r_{in} + r_{o}) + 1
\]

Where, 

- \( k \): sense gain products error amp. gain,
- \( \text{PWM} \): gain of the comparator.

In open loop case, the peak frequency is the same resonant frequency \( f_p \) of the loop gain \( T(s) \) as shown in Fig. 5, and the peak value of the output impedance can be derived from Eq. (4).

\[
\text{From Eq. (2), the low-frequency value of input impedance } |Z_{in}(0)| \text{ is given by following equation.}
\]

\[
\left| Z_{in}(0) \right|_{dB} \approx 20 \log \left( \frac{R + r_{e}}{D^2} \right) \quad (dB\Omega) \tag{3}
\]

\[|Z_{in}(0)|\] has minimum value at rated load, so the estimation of \( |Z_{in}(0)| \) must be at rated load. Next, the output impedance is examined.

#### B. Output Impedance

The output impedance of bus converter can be derived as following equations.

\[
Z_o(s) = \frac{Z_b(s)}{1 + T_b(s)} \tag{5}
\]

\[
Z_o(s) = \frac{s^2 L_b C_b r_{in} + s \left( L_b + C_b r_{in} + r_o \right) + r_{in}}{s^2 L_b C_b + s \left( r_{in} + r_o \right) + 1}
\]

In open loop case, the peak frequency is the same resonant frequency \( f_p \) of the loop gain \( T(s) \) as shown in Fig. 5, and the peak value of the output impedance can be derived from Eq. (4).

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\]

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\]
In closed loop case, the output impedance peak moves to crossover frequency $f_c$ as shown in Fig. 5. In this instant the peak value of the closed loop output impedance can be derive following equation.

$$Z_{\text{oc, peak}} = \frac{L_0}{C_0 \left( r_c + r_i \right)} \quad (9)$$

where,

$$\alpha = \left[ \mathcal{F}(0) \right] = k \cdot PWM \cdot V_i$$ \hspace{1cm} (11)

Moreover, from transfer function of loop gain, the crossover frequency $f_c$ is expressed as follows by means of peak frequency $f_p$ of loop gain.

$$f_c = \sqrt{1 + \alpha f_p} \quad (12)$$

From Eq. (10) (12), the peak value of closed loop output impedance is expressed as follows.

$$Z_{\text{oc, peak}} = \frac{L_0}{C_0 \left( \frac{f}{f_p} r_c + r_i \right)} \quad (13)$$

As shown in Eq. (13), if $f_c$ is equal to $f_p$, it becomes the same as Eq(9). Therefore, the peak value of output impedance is calculable by means of Eq. (13).

**IV. OUTPUT IMPEDANCE SPECIFICATION**

The output impedance characteristic of each control shames is different, and each bus converter has different operation. Therefore, the output impedance design suitable for the feature of each control method is required. From now, the output impedance design for each control shames is considered.

**A. Un-regulated**

In un-regulated case, the output impedance is the same as open-loop output impedance because of this control method has no control loop. In order to reduce the peak value of output impedance, it is effective to make inductance small or to enlarge capacitance.

Generally, un-regulated bus converter is operated at maximum duty ratio. Therefore, the inductor of the bus converter can be reduced as small as possible to reduce the system instability. The peak value of output impedance is reducing with small inductor. Figure 6 shows the experimental result of the relation between the output impedance and inductance. Moreover, Fig. 7 shows the analytical and experimental results of the relation between the peak value of output impedance and inductance. Both results agreed well. As mentioned above, the peak of impedance is easily obtained from Eq. (13). However, this method depends on converter topology that has a double-ended circuit at secondary side such as half-bridge or full-bridge. Moreover, there are some limits such that high accurate input voltage or a POL with wide input range.

**B. Semi-regulated**

Semi-regulated bus converter has a control loop. However, regulation is related to variation of input voltage, therefore the output impedance is same as un-regulated case. In this case, the duty ratio is changed, and the inductor of the bus converter cannot be reduced. Therefore, very large bus capacitor is needed to reduce the peak value of output impedance.

Figure 8 shows the experimental result of the relation between the output impedance and capacitance. Moreover, Fig. 9 shows the analytical and experimental results of the relation between the peak value of output impedance and capacitance. Both results agreed well.
In semi-regulated case, essentially it becomes very unstable and we have found that the demerit is very large capacitors are needed at the intermediate bus in order to be stable. However, it can be used at limited conditions such as wide input range (36-75V) and POL with low power (in other words, POL with very high input impedance).

C. Full-regulated

Full-regulated bus converter has a feedback loop, so the output impedance characteristic is changed. Therefore, output impedance can be made small with wide bandwidth. Figure 10 shows the experimental result of the relation between the output impedance and bandwidth. Moreover, Fig. 11 shows the analytical and experimental results of the relation between the peak value of output impedance and bandwidth. Both results agreed well.

Next, the relation between capacitance and output impedance peak is examined in closed loop case. In closed loop case, if capacitance $C_b$ changes to $C_b + C_{add}$, peak frequency $f_p$ of loop gain is changed as follows.

\[ f_p' = \frac{1}{2\pi \sqrt{L_b (C_b + C_{add})}} \]  \hspace{1cm} (14)

Therefore, the crossover frequency $f_c$ is changed as follows.

\[ f_c' = \sqrt{1 + \alpha} f_p' \]  \hspace{1cm} (15)

Moreover, frequency ratio $f_c' / f_p'$ is given as following equation.

\[ \frac{f_c'}{f_p'} = \frac{f_c}{f_p} \]  \hspace{1cm} (16)

From these results, output impedance peak can be expressed as following equation.

\[ Z_{oc\_peak} = \frac{k_c C_b}{C_b + C_{add}} Z_{oc\_peak} \]  \hspace{1cm} (17)

where, $k_c$

\[ k_c = \frac{(1 + \alpha) r_{ch} + r_{lb}}{(1 + \alpha) r_{ch} + r_{lb}} \]  \hspace{1cm} (18)

Figure 12 shows the experimental result of the relation between the output impedance and capacitance in closed loop case. Moreover, Fig. 13 shows the analytical and experimental results of the relation between the peak value of output impedance and capacitance in closed loop case. Both results agreed well. In this case, the total ESR is greatly changed by the additional capacitor. Moreover, in the case of closed loop, ESR has a great influence to the output impedance peak. Therefore, estimation of ESR is very important.

V. OPTIMAL DESIGN OF BUS CONVERTER

In order to evaluate the performance of this system, the experiment circuits are implemented using the specifications and parameters in Table 1.
Here, the case with two POLs is discussed for actual example. The practical design process is shown below.

A. Input impedance estimation

The low-frequency value \(|Z_{in}(0)|\) of input impedance is given by Eq. (3). The duty ratio is \(D=0.275\) and output resistance is \(R=0.66(\Omega)\) from the relation input and output. In this case, the \(|Z_{in}(0)|\) is 20.6(dBΩ).

When two POLs of same condition are connecting in parallel, \(|Z_{in}(0)|\) is 14.6(dBΩ). Figure 14 shows the experimental result of input impedance. The low-frequency value \(|Z_{in}(0)|\) is around 15(dBΩ) as shown in Fig. 14.

The experimental results and analytical results are agreed well. If the stability margin is set to 6(dBΩ), then the peak value of output impedance must be set to 8.6(dBΩ).

B. Output impedance design

Figure 15 shows the output impedance characteristic of the basic case using the parameter of Table I. As shown in Fig. 15, the peak value of the output impedance is around 18(dBΩ). From mentioned above calculation, the peak value of the output impedance needs to set around 8.6(dBΩ) for sufficient system stability.

In un-regulated case, the optimal inductance value is considered because the stability is improved by small inductance. From Eq. (13), the optimal inductance value can be derived as following equation.

\[
L_{o,\text{optimal}} = \frac{C_{\text{o}}}{(r_{\text{i}} + r_{\text{o}})} \left( Z_{o,\text{peak}} \right) \tag{19}
\]

where, the unit of \(|Z_{o,\text{peak}}|\) is Ω.

Since the output impedance must be set to 8.6(dBΩ), the inductance value is set to around 87(μH) from Eq. (19). Figure 16 shows the experimental result of the output impedance with small inductance.

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<th>Symbol</th>
<th>Description</th>
<th>Value</th>
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<tr>
<td>Vin</td>
<td>Input Voltage</td>
<td>48V</td>
</tr>
<tr>
<td>Vb</td>
<td>Bus Volotage</td>
<td>12V</td>
</tr>
<tr>
<td>Lb</td>
<td>Output Inductor of Bus Converter</td>
<td>270μH</td>
</tr>
<tr>
<td>Cb</td>
<td>Output Capacitor of Bus Converter</td>
<td>100μF</td>
</tr>
<tr>
<td>rlb</td>
<td>Resistance of Lb</td>
<td>300mΩ</td>
</tr>
<tr>
<td>reb</td>
<td>ESR of Cb</td>
<td>25mΩ</td>
</tr>
<tr>
<td>kb</td>
<td>Feedback gain (with sensing gain)</td>
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</tr>
<tr>
<td>Vo/Io</td>
<td>Output Condition</td>
<td>3.3V/5A</td>
</tr>
<tr>
<td>Lo</td>
<td>Output Inductor</td>
<td>2.8μH</td>
</tr>
<tr>
<td>Co</td>
<td>Output Capacitor</td>
<td>820μF</td>
</tr>
<tr>
<td>rl</td>
<td>Resistance of Lo</td>
<td>25mΩ</td>
</tr>
<tr>
<td>re</td>
<td>ESR of Co</td>
<td>10mΩ</td>
</tr>
</tbody>
</table>

Fig. 12. Additional capacitance and output impedance

Fig. 13. Additional capacitance and peak value of Zo

Fig. 14. Input impedance characteristic.
The inductance value is around 90 (\(\mu\)H), and the peak value of output impedance is around 8.5 (dB\(\Omega\)). The experimental results and analytical results are agreed well. Moreover, in open loop case, since the \(r_L\) is generally larger than \(r_c\), the output impedance does not become smaller than \(r_L\) as shown in Fig. 6. Therefore, the inductance value has minimum value. From Eq. (19), the minimum value of the inductance is given by following equation.

\[ L_{\text{min}} = C_s \left( r_c + r_{\text{esr}} \right) r_c \quad (20) \]

In this case, the minimum value of inductance is around 10 (\(\mu\)H).

In semi-regulated case, the optimal capacitance value is considered because the stability is improved by large capacitance. From Eq. (13), the optimal capacitance value can be derived as following equation.

\[ C_{\text{optimal}} = \frac{L_{\text{opt}}}{(r_c + r_{\text{esr}}) Z_{\text{esr, peak}}} \quad (21) \]

where, the unit of \(Z_{\text{esr, peak}}\) is \(\Omega\). Since the output impedance must be set to 8.6(dB\(\Omega\)), the capacitance value is set to around \(300(\mu\)F) from Eq. (16). In this case, the influence of ESR is considered. Because the ESR becomes small when the capacitor is connected in parallel.

Figure 17 shows the experimental result of output impedance with large capacitance. The capacitance value is 300 (\(\mu\)F), and the peak value of output impedance is around 8 (dB\(\Omega\)). The experimental results and analytical results are agreed well.

Moreover, the output impedance does not become smaller than \(r_L\) as shown in Fig. 8. Therefore, the capacitance value has maximum value. From Eq. (21), the maximum value of the capacitance is given by following equation.

\[ C_{\text{max}} = \frac{L_s}{(r_c + r_{\text{esr}}) r_c} \quad (22) \]

In this case, the maximum value of capacitance is around 2.8 (mF).

In full-regulated case, the optimal bandwidth is considered because the stability is improved by wide bandwidth. From Eq. (13), the optimal bandwidth can be derived as following equation.

\[ f_{\text{optimal}} = f_p \sqrt{\frac{L_{\text{opt}}}{C_{\text{optimal}} Z_{\text{esr, peak}}} - r_s r_c} \quad (23) \]

where, the unit of \(|Z_{\text{esr, peak}}|\) is \(\Omega\). Since the output impedance must be set to 8.6(dB\(\Omega\)), the bandwidth is set to around 5.1kHz from Eq. (23). Figure 18 shows the experimental result of the output impedance with wide bandwidth. The bandwidth is around 4.7kHz, and the peak value of output impedance is around 8.5 (dB\(\Omega\)). The experimental results and analytical results are agreed well.

Next, the optimal capacitance is considered in closed loop case. From Eq. (17), the optimal additional capacitance can be derived as following equation.

\[ C_{\text{add, optimal}} = \frac{k_{\text{esr}} Z_{\text{esr, peak}}}{Z_{\text{esr, peak}}} - 1 \cdot C_b \quad (24) \]

The basic parameters case, the closed loop output impedance peak is around 14.5(dB\(\Omega\)). Since the output impedance must be set to 8.6(dB\(\Omega\)), the additional capacitance is set to around \(150(\mu\)F) from Eq. (24). Figure 19 shows the experimental result of the output impedance with additional capacitance. The capacitance is around 150\(\mu\)F, and the peak value of output impedance is around 9 (dB\(\Omega\)). The experimental results and analytical results are agreed well.
VI. CONCLUSIONS

This paper presents the output impedance design for on-board distributed power system by means of three control methods of bus converter. The output impedance peak of the bus converter and the input impedance of the POL were analyzed, and it was confirmed by experimentally for stability criterion. As a result, the standard of the discrimination of stability on a frequency response of input and output impedance was clarified. Furthermore, the design process of each control method for system stability was proposed.

![Graph showing output impedance with additional capacitance](image)

Fig. 19. Output impedance with additional capacitance

REFERENCES


