Input Current-Ripple Consideration for the Pulse-link DC-AC Converter for Fuel Cells by Small Series LC Circuit

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Abstract—This paper mentions the input current ripple reduction method of the Pulse-link DC-AC Converter for Fuel Cells. The conventional DC-AC converter for fuel cells is interpolated large capacitor between boost converter stage and PWM inverter stage. That capacitor disturbs the size reduction of this unit. To overcome this problem, authors have proposed a novel topology called as Pulse-link DC-AC converter. The proposed topology provides boosted-voltage pulse directly to PWM inverter. This topology does not require large capacitor between two stages. Instead, small values of inductor and capacitor are connected series and inserted between two stages in parallel. This paper examines the relationship between the inductor and capacitor values and input current-ripple. As the result, inductor value has the relationship with current-ripple.

I. INTRODUCTION

In recently years, energy consumption problem such as global heating has become a huge international problem. In Japan, about 30% of amount of CO₂ emission is produced by energy conversion department [1]. Therefore, some new clean energy system is required strongly. One of the new clean energy system using fuel cells has been collecting global interests. When fuel cells generate electricity, a large amount of thermal energy arises at the same time. So, the cogeneration system using both electricity and thermal energy is now researched actively around the world. In particular, a home-use cogeneration system with fuel cells is developed from the stream of what is called distributed power system or micro-grid power systems. When cogeneration system is set near home, the distribution loss can be reduced. Now, home power source is AC. On the other hand, the voltage provided by fuel cells is DC. Therefore, a DC-AC converter is essential for the home-use cogeneration system.

The specifications for DC-AC converter for fuel cells have 3 terms – 1) boost, 2) isolation, and 3) low current-ripple. The voltage from fuel cells is DC, and is generally lower than commercial voltage. Therefore, DC-AC converter boosts input voltage from fuel cells to the level of commercial voltage. On the point of safety, DC-AC converter has isolation structure between fuel cells stage and load stage. Third-term is special term for fuel cells application. Current-ripple in fuel cells is serious problem. The current-ripple in fuel cells gives damage to the fuel capacity and life span because chemical reaction time is much slower than commercial frequency [2, 3, 4]. Therefore, DC-AC converter should reduce input current-ripple.

The conventional DC-AC converter construction for fuel cells is shown in Fig. 1. The conventional topology is constructed two stages – first stage is isolated boost DC-DC converter and second stage is PWM inverter. And between two stages, a large smoothing capacitor is connected in parallel. This capacitor works as smoothing output voltage, and it also works as reducing input current-ripple. This capacitor absorbs the variation from AC. However, this capacitor disturbs the size reduction of this unit.

To overcome above problem, authors have proposed a novel DC-AC converter called as Pulse-link shown in Fig. 2 [5]. In this topology, the first-stage boost converter provides a series boosted voltage pulses directly to the second-stage PWM inverter. Therefore, a large smoothing capacitor is not needed. This concept has known as high frequency link or pulse DC link [6, 7]. However, [6,7] do not mention about current-ripple. Authors have suggested that a series connected LC circuit is inserted in parallel between two stages in order to reduce current-ripple.

Furthermore, authors suggested the input current-ripple reduction method that resonant frequency of series LC circuit is adjusted the twice of commercial frequency [8]. The result of reduction was good, but the inductance value became large.

To reduce the values more, this problem, this paper examines the parameter values of inductor and capacitor which are not so large.
II. STEADY-STATE CHARACTERISTICS

A. Topology and operation states

Fig. 2 shows the pulse-link circuit topology. As mentioned above, this topology has two stages, and this converter provides boosted pulsed voltage directly to PWM inverter. And between two stages, series LC circuit is connected in parallel in order to reduce current-ripple. The value of the capacitor using this LC circuit is less than the conventional one. Fig. 3 shows the switching sequences model of this converter in commercial frequency. This converter has 5 switches. Switch Q1 controls the boost pulse from input voltage. And, from S1 to S4 are PWM inverter switches. S1 and S4 are controlled to make output voltage sinusoidal waveform, while S2 and S3 are decided the plus/minus of output voltage. And control combination of S1, S3 and S2, S4 is operated in the same time. Q1 and S1/S4 are synchronous at rising time. Here, the steady-state characteristics are analyzed in switching period. In analysis, output voltage is positive semicircle period. As the result, there are three states in one switching period. Fig. 4 shows the equivalent circuits of each state.

B. Steady state analysis

From those equivalent circuits, the steady-state characteristics are calculated. The steady-state equations are written below:

\[ V_c = \frac{n}{1-D_{Q1}} V_i \]  \hspace{1cm} (1)

\[ V_o = \frac{n d_i(t)}{1-D_{Q1}} V_i \] \hspace{1cm} (2)

Furthermore, from equation (1), the peak voltage pulse that is input to PWM inverter \( V_{\text{inv-in}} \) is written below:

\[ V_{\text{inv-in}} = \frac{n}{1-D_{Q1}} V_i \] \hspace{1cm} (3)

Here, \( D_{Q1} \) is duty ratio of switch Q1. And, \( d_i(t) \) is duty ratio of PWM inverter switch of S1/S4. \( d_i(t) \) is changed shown as equation (4) in order to make output voltage to be sinusoidal waveforms.

\[ d_i(t) = d_{i_{\text{max}}} \left| \sin(2\pi \cdot f \cdot t) \right| \] \hspace{1cm} (4)

Moreover, the relationship of \( D_{Q1} \) and \( d_{i_{\text{max}}} \) is limited equation (5), because PWM inverter is provided voltage only when Q1 is ON.

\[ D_{Q1} \geq d_{i_{\text{max}}} \] \hspace{1cm} (5)

C. Experimental results

To evaluate the performance of the circuit, the experimental circuit is implemented with the specifications and parameters in Table 1. From table 1, \( C_1 \) is 3 mF, and it is aluminum electrolytic capacitor. \( C_1 \) is decided from the allowable current. Primary-side is flown large current, so capacitance of \( C_1 \) becomes large value. However, primary-side is low voltage, so the size of aluminum electrolytic capacitor is not so large even if the value is large because withstand-voltage is low. Therefore, large value of aluminum electrolytic capacitor is used at \( C_1 \) in this experiment.

Fig. 5 shows the characteristics of efficiency vs. output power. Here, input voltage is constant value 20 V, and output voltage is regulated \( V_{1100} \). From fig. 5, it is considered that the efficiency is more than 90 %. This topology achieves to convert DC to AC with high efficiency.
Fig. 4. Equivalent circuits of each state.

a. State 1 \((Q_1: \text{ON}, \ S_1: \text{ON}, \ S_3: \text{ON})\).

b. State 2 \((Q_1: \text{ON}, \ S_1: \text{OFF}, \ S_3: \text{ON})\).

c. State 3 \((Q_1: \text{OFF}, \ S_1: \text{OFF}, \ S_3: \text{ON})\).

Fig. 5. Characteristics of Efficiency vs. Output power.

Fig. 6. Experimental waveforms of output voltage \((v_o)\), input current \((i_i)\), and inductor current of \(L_2\) \((i_{L2})\) when output power is 100 W. For the comparison, the experimental waveforms when series \(L_2C_3\) circuit is not inserted are shown in fig. 7. The output load condition is same. When \(L_2C_3\) circuit is not inserted in the topology, input current-ripple is 6.11 Ap_p.

### III. PREVIOUS CURRENT–RIPPLE REDUCTION METHOD

Input current-ripple is occurred by output commercial AC output voltage. The frequency of input current-ripple is 100 Hz when the frequency of output voltage is 50 Hz, because this converter switches plus/minus side of commercial voltage by controlled \(S_2/S_3\) switches timing.

If the resonant frequency of series \(L_2C_3\) circuit connected the circuit in parallel is synchronized 100 Hz, input current-ripple will be reduced. Impedance of series \(L_2C_3\) circuit is written below equation:

\[
|Z| = \left| \frac{\omega L_2 - \frac{1}{\omega C_3}}{\omega C_3} \right| \tag{10}
\]

Capacitor is not recommended large capacitance value, here inductance is being changed.

### TABLE I. CIRCUIT PARAMETER VALUES

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_i)</td>
<td>Input voltage</td>
<td>20[V]</td>
</tr>
<tr>
<td>(L_1)</td>
<td>Input inductance</td>
<td>400[uH]</td>
</tr>
<tr>
<td>(L_2)</td>
<td>Middle inductance</td>
<td>1[mH]</td>
</tr>
<tr>
<td>(L_M)</td>
<td>Magnetizing inductance</td>
<td>400[uH]</td>
</tr>
<tr>
<td>(C_1)</td>
<td>primary-side capacitance</td>
<td>3[mF]</td>
</tr>
<tr>
<td>(C_2)</td>
<td>Secondary-side capacitance</td>
<td>330[uF]</td>
</tr>
<tr>
<td>(C_3)</td>
<td>Middle capacitance</td>
<td>300[uF]</td>
</tr>
<tr>
<td>(n)</td>
<td>Turn ratio</td>
<td>3</td>
</tr>
<tr>
<td>(L_0)</td>
<td>Output inductance</td>
<td>3[mH]</td>
</tr>
<tr>
<td>(C_0)</td>
<td>Outout capacitance</td>
<td>9.4[uF]</td>
</tr>
<tr>
<td>(f_s)</td>
<td>Switching frequency</td>
<td>30[kHz]</td>
</tr>
</tbody>
</table>

Fig. 7 shows the characteristics of series \(L_2C_3\) impedance and input current-ripple measurement by changing of \(L_2\). Here, the value of \(C_3\) is 300 uF, and \(\omega = 2 \cdot \pi \cdot 100 \text{ rad/s}\). From fig. 8, it is considered that impedance \(|Z|\) curve and experimental measurement of input current-ripple is agreed well.

Fig. 8 shows the characteristics of series \(L_2C_3\) impedance and input current-ripple measurement by changing of \(L_2\). Here, the value of \(C_3\) is 300 uF, and \(\omega = 2 \cdot \pi \cdot 100 \text{ rad/s}\). From fig. 8, it is considered that impedance \(|Z|\) curve and experimental measurement of input current-ripple is agreed well.
Furthermore, the experimental waveforms at $L_2=8 \text{ mH}$ is shown in fig. 9. From fig. 8, inductor current of $L_2$ is oscillated with opposite phase of output semi-sinusoidal voltage. This thing means that when output load is light, extra energy from input power is stored by series $L_2C_3$, and when output power is heavy, series $L_2C_3$ provides with input power. From the result, this series $L_2C_3$ circuit is regarded as pulse energy tank, and works as ripple canceling circuit.

**IV. PROPOSED CURRENT–RIPPLE REDUCTION METHOD**

Previous chapter mentioned the ripple reduction method adjusting the resonant frequency. However, this method has the drawback. The inductor value of $L_2$ has become large value because adjusting frequency is low. As the result, it is not easy to take off the size of this unit. Therefore, this method is not the best way to reduce current-ripple.

Here, it examines the relationship of inductance and capacitance of $L_2$ and $C_3$ with input current-ripple reduction.

**A. Capacitance $C_3$**

Firstly, it examines the effect on the capacitance $C_3$ for current-ripple. Here, inductance $L_2$ is 300$\mu$H. Circuit parameters values are same as Table I, and output resistance is constant as $100\Omega$. Fig. 10 shows the experimental measurement. From the result, it is considered that as capacitance value is increased, current-ripple becomes large.

Furthermore, the scale of the values is logarithm scale. And, there is a bottom value when $L_2$ is 40$\mu$F. Therefore, at next chapter, capacitance $C_3$ is set as 40$\mu$F. This value is able to be used film-capacitor.

**B. Inductance $L_2$**

Secondly, it examines the relationship of inductance for current-ripple. Mentioned previously, $C_3$ is 40$\mu$F. Experimental measurement is shown in Fig. 11. From the result, it is considered that the current-ripple is rising at more than 400$\mu$H, while the current-ripple is small at less than 400 $\mu$H. Furthermore, it is observed that output voltage is almost constant from 400$\mu$H and more, while output voltage is increasing at less than 400$\mu$H.

Fig. 12, 13 show the experimental waveforms of input PWM inverter voltage $v_{inv_in}$ and inductor current of $L_2$ $i_{L2}$. Fig. 12 is at $L_2=200$ $\mu$H, and fig. 13 is at $L_2=700$ $\mu$H. From these results, the boundary point is the turning point when $i_{L2}$ has flat period in one switching period- that seems to be the boundary of CCM and DCM. Furthermore, it is considered that input current-ripple is reduced when $i_{L2}$ has flat period like at DCM.

Fig. 14 shows the experimental waveforms of $v_o$ and $i_i$ at the least ripple value when $L_2$ is 300$\mu$H and $C_3$ is 40$\mu$F. From the waveforms, it is observed that input current is almost flat and ripple is less than previous method.

From those results, the new method of reduction ripple is suggested. It chooses the parameter that inductor current of $L_2$ has flat period in one switching period, current-ripple will be reduced. This method can be achieved smaller values. Therefore, it may reduce the size of this unit.
V. CONCLUSION

Finally, we mention the conclusion. This paper mentioned the input current-ripple methods for DC-AC converter. Previous method is able to reduce ripple, but it has drawback about values. This paper examined the effect on current-ripple reduction by using small inductance \( L_2 \) and capacitance \( C_3 \). Capacitance can be used less than 50\( \mu \)F, which is able to be used film-capacitor. When inductor current of \( i_2 \) has flat period in one switching period, the ripple-current is reduced. This method is achieved that ripple-current is less than previous one, and parameter values are also reduced.

REFERENCES


