Dynamic Characteristics of DC-DC Converter with Novel Digital Peak Current-Injected Control

Fujio Kurokawa¹, Junya Sakemi¹, Shohei Sukita¹, Yuichiro Shibata¹, Masato Soejima¹, Tomonori Yokoyama², Masahiro Sasaki³ and Yasuhiro Mimura³

¹ Nagasaki University, 1-14 Bunkyo-machi, Nagasaki, 852-8521 Japan
² Tokyo Denki University, 2-2 Kandanishiki, Chiyoda-ku, Tokyo, 101-0054 Japan
³ Shindengen Electric Mfg. Co., Ltd., Hanno-shi, 357-8585 Japan
E-mail: fkurokaw@nagasaki-u.ac.jp

Abstract —This paper presents the dynamic characteristics of the proposed digital control current mode dc-dc converter. In the proposed novel digital control circuit, the peak current-injected control is realized using the combination of the simple dual A-D signal converter and the programmed delay circuit. In 100kHz digitally controlled dc-dc converter, it is seen in simulation that the proposed method has no overshoot of the output voltage and the convergence time that the output voltage is settled to steady-state is only 151μs. The difference between the transient time of the proposed circuit and that of the conventional method is an order of magnitude. Furthermore, the ratio of resolution of the DPWM generator against the output voltage is 0.27% and is satisfied to apply the commercial power supply unit.

I. INTRODUCTION

The telecommunications and data communications systems consist of the telecommunications equipment, data communications equipment, data transmitter/receiver, power supply and so forth in the communications building. Recently, in this field, the power supply system requires the high performance characteristics, high energy management function, smart networking function, high reliability and small size more. However, since the power supplies are usually controlled by the analog circuit, it is difficult to solve these problems. Therefore, the digital control techniques have been growing to apply to these switching power supplies [1]-[5]. The central research target of digital control circuit is to improve the dynamic characteristics because the conversion time of the A-D converter and the processing time of the digital controller exert a bad influence upon the dynamic characteristics. In this case, we think that two solutions are considered. One solution is to add the feedforward control loop and digital peculiar circuit [6]. Another solution is to add the other feedback control loop and also digital peculiar circuit. Not only the output voltage but also input voltage, switch/reactor current or/and output current are detected to perform these controls as shown in Fig. 1. Conventionally, it seems that the feedback loop has the disadvantage because there is essentially a delay time in the digital control. At an example, the current mode dc-dc converter is useful in order to perform the superior dynamic characteristics. However, these studies have focused on sensing the delayed average value of the switch/reactor current because it is very difficult to sample the data of accurate peak point of switch/reactor current at the real time. Therefore, it has been reported that the peak point is estimated from the slope of reactor current, but there has been no study that tried to detect the peak value of reactor-switch current at real time.

This paper presents the dynamic characteristics of proposed novel digital control dc-dc converter [7] which is able to detect the peak switch current of the high frequency switching dc-dc converter at real time. In this proposed digital control circuit, the peak current-injected control is realized using the combination of the simple dual analog-to-digital signal converter and the programmable delay circuit.

II. CIRCUIT CONFIGURATION AND OPERATION PRINCIPLE

Figure 2 shows the configuration of proposed future digital power supply and monitoring system to increase the reliability of the telecommunications and data communications equipment in the communications building. In this system, all switching power supplies are controlled by the monitor station and the energy can be saved easily. The data of not only telecommunications and communications equipments but also power supply are transferred to the remote operation center in detail via the data transmitter/receiver.
Figure 3 shows the circuit configurations of digitally controlled dc-dc converter. In this circuit, $E_i$ is the input voltage, $e_o$ is the output voltage, $i_o$ is the output current, $D$ is the fly wheel diode, $C$ is the output smoothing capacitor, $R$ is the load, $L$ is the energy storage reactor, $T_r$ is the main switch, $i_{Tr}$ is the switch current and $E_o^*$ is the constant reference voltage. The switch current $i_{Tr}$ is detected as the voltage $e_s$ by a sensing resistor $R_s$. The output voltage $e_o$ and the switch current $i_{Tr}$ are detected and are sent to the digital control circuit as shown in Fig. 4.

Figure 4 shows the proposed high performance digital control circuit which will be used in the near future system as shown in Fig. 2. The function of this circuit is divided into the average voltage detector and peak current detector. The average voltage detector is composed of the pulse code analog-to-digital (PC A-D) converter #1, PC A-D converter #2, Counter #1, Counter #2 and PID control portion. $S_{vsam}$ is the clock pulse. $S_1$ and $S_2$ are signal against the output voltage $e_o$ and the constant reference voltage $E_o^*$, respectively. $N_{RM}$ is the calculated results in the PID control portion. The peak current detector is composed of the PC A-D converter #3, PC A-D converter #4, programmable delay circuit and DPWM generator. $S_{csam}$ is the clock pulse. $S_{csam}^*$ is the delayed signal by $S_{csam}$. $E_c$ is the constant voltage against the peak current. $e_s$ is the voltage against the switch current $i_{Tr}$. $S_{es}$ and $S_{ep}$ are signal against $e_s$ and $E_c$. $S_{on}$ is signal against the on time of the main switch $T_r$.

For example, the configuration of the PC A-D converter #1 is shown in Fig. 5. The PC A-D converter consists of the CR integrator and transistor switch to reset the ramp voltage. The configuration is very simple. Moreover, as shown in Fig. 4, since the dual PC A-D converter is used in the average voltage detector and the peak current detector, respectively, the influence of temperature, noise and so forth are rejected.

The configuration of a programmable delay circuit is shown in Fig. 6. The delay buffers #1–#3 are performed to generate the programmed delay signal $S_{csam}^*$ by $N_{RM}$. This $N_{RM}$ is the output value of the calculated result with PID control portion.

Figure 7 shows operation principle of the dual PC A-D converter in average voltage detector. In this figure, $S_{vsam}$ is the clock pulse and $S_{TS}$ is the start signal corresponding to the switching period, the output voltage $e_o$ of dc-dc converter and the constant reference voltage $E_o^*$ are converted into the Ramp Voltage #1 and Ramp Voltage #2. They are compared with the threshold voltage $V_{thv}$ of PC A-D converter #1 and #2, and converted into $S_1$ which is corresponding to the Ramp voltage #1 and $S_2$ which is corresponding to the Ramp voltage #2. In addition, $S_1$ is counted by the Counter #1, and converted into $N_{eo}$. $N_{eo}$ is represented as follows:

$$N_{eo} = S_{vsam} \frac{e_o}{e_o - V_{thv}} \frac{\tau_v}{(e_o - V_{thv})} (1)$$

where $\tau_v$ is the time constant of CR integrator. Moreover, $E_o^*$ is converted into the $N_{E_o^*}$ as well as $N_{eo}$. 

The difference of these values is calculated by the PID control portion. The output value $N_{RM}$ of the calculated result with PID control portion is sent to the delay circuit and this calculated result $N_{RM}$ decides the delay time $T_D$ of programmable delay circuit as shown in Fig. 6.

$$T_D = T_{DSEL} N_{RM}$$  \hspace{1cm} (2)

where $T_{DSEL}$ is the delay time of each delay buffer shown in Fig. 6.

Figure 8 shows operation principle of dual PC A-D converter in peak current detector. $S_{csam}$ is the clock pulse. $T_D$ is Eq. (2). $t_{Ec}$ is time when the ramp voltage #4 reaches the threshold voltage $V_{thc}$. The delayed signal $S_{csam}^*$ of the programmable delay circuit generates the start signal of the ramp voltage #4 of PC A-D converter #4 during each divided short period $T_{SD}$ of the switching period $T_s$. The ramp voltage #4 is increased from this point of time and the pulse signal $S_{ep}$ is generated when it reaches the threshold voltage $V_{thc}$. The ramp waveform is generated by the simple CR integrator as shown in Fig. 5 and the ramp voltage #4 is corresponding to the constant voltage $E_c$ in the PC A-D convert #4 of peak current detector. In the PC A-D converter #3, the ramp voltage #3 corresponding to the switch current $i_{Tr}$ is increased during each divided period $T_{SD}$ and $S_{es}$ is generated as well as $S_{ep}$. In this case, the start time has no delay against the clock pulse $S_{csam}$.

Figure 9 shows operation principle of peak current detector. When $e_s$ is larger than the constant voltage $E_c$, $S_{es}$ is generated at the early time against $S_{ep}$ during some divided period $T_{SD}$. At the same instant, the signal of the digital PWM (DPWM) generator directs the main switch $T_r$ to turn off and the signal $S_{on}$ against the on time interval $T_{on}$ is decided.

As a consequence, the peak current-injected control is realized by the simple A-D converter and programmable delay circuit.

### III. RESOLUTION OF OUTPUT VOLTAGE

Next, the resolution against the output voltage of the DPWM generator will be discussed.

In Figs. 6 and 9, $T_D$ is represented as follows;

$$T_D = T_{DSEL} \left[ N_B - K_P (N_{eo} - N_{eo^*}) - K_I \sum N_I - K_D N_D \right]$$  \hspace{1cm} (3)

where $N_B$ is bias value, is the desired value $N_{eo^*}$ in the P control and $K_P$ is the proportional coefficient, respectively. $N_D$ is multiplied by the differential coefficient $K_D$ and $K_D$ $N_D$ is generated at the multiplier. $\Sigma N_I$ is also multiplied by the integral coefficient $K_I$. In this case, $N_{INT}$ is the predetermined reference value in the I control and corresponds to the desired output voltage of the dc-dc converter.

When the ramp voltage #4 reaches the threshold voltage $V_{thc}$, the following relation is obtained.
\[ t_{E_c} = t(E_c) = \tau_c \ln \left( \frac{E_c}{E_c - V_{thc}} \right) \]  \hspace{1cm} (4)

Assuming that the small variation \( \Delta e_{pv} \) of the peak value \( e_p \) of Ramp voltage #3 is caused at the voltage \( E_c \), the following equation is obtained:

\[ \Delta e_{pv} = -\left( \frac{E_c}{V_{thc}} - 1 \right) \frac{E_c \bar{T}DSEL}{\tau_c} \Delta N_R = -K_{DA} \Delta N_R \]  \hspace{1cm} (5)

where

\[ K_{DA} = \left( \frac{E_c}{V_{thc}} - 1 \right) \frac{E_c \bar{T}DSEL}{\tau_c} \]  \hspace{1cm} (6)

where \( \tau_c \) is the time constant of CR integrator.

In Fig. 8, the following relation is obtained because the peak value \( e_p \) of ramp voltage #2 is corresponding to \( e_s \).

\[ \frac{T_{on}}{T_s} = \frac{2f_s L}{A_{cc} R_s (E_i - E_o)} \left( e_p - A_{cc} R_s I_{Tr} \right) \]  \hspace{1cm} (7)

where \( A_{cc} \) is the gain of amplifier of current detector and \( f_s \) is the switching frequency.

In the DC-DC converter in Fig. 3, assuming that the small variation \( \Delta E_o \) in \( E_o \) and \( \Delta T_{on} \) in \( T_{on} \) are caused by the small variation \( \Delta I_o \) in \( I_o \), the following equation is obtained:

\[ \Delta E_o = \frac{\Delta T_{on}}{T_s} E_i - r \Delta I_o \]  \hspace{1cm} (8)

where \( r \) is the internal loss of the dc-dc converter.

Considering Equations (5), (7) and (8), the following equation is represented, the resolution of the DPWM generator against the output voltage is obtained as follows;

\[ \frac{\Delta E_o}{\Delta N_{RM}} = \frac{2f_s L E_i}{1 + \frac{r}{R}} A_{cc} R S \left( E_i - E_o \right) + 2f_s L E_i A_{cc} \frac{R S}{R} K_{DA} \]  \hspace{1cm} (9)

IV. SIMULATED RESULTS

Figures 10 and 11 show the simulated transient response of the conventional and proposed control dc-dc converters in step change of the load resistor \( R \) from 10Ω to 5Ω, taking \( K_I \) as parameter. The simulator is PSIM. The switching frequency is 100kHz, \( L \) is 188μH, \( C \) is 100μH and \( E_i \) is 20V.

In Figs. 10(a) through (c), the superior transient response of conventional circuit is obtained in case of \( K_I = 0.01 \) as shown in Fig. 10(b). The undershoot of output voltage, the overshoot of reactor current and transient time of the output voltage are over than 6.0%, 42% and 1,016μsec, respectively. It is not so good characteristics because there is no current detector in Fig. 4. The transient time is too long and the overshoot of reactor current is large.
In Figs. 11(a) (b) and (c), the circuit parameters are the same as those of Fig. 10. The superior transient response of proposed circuit is obtained in case of $K_I=0.18$ as shown in Fig. 12(b). The undershoot of output voltage, the overshoot of reactor current and transient time of the output voltage are less than 2.8%, 18% and 151 μsec, respectively. When $K_I$ is equal to 0.4, it is seen that the difference between the transient time of the proposed circuit and that of the conventional method is two orders of magnitude.

Figure 12 shows the relationship between the resolution of the DPWM generator and time-delay $T_{\text{DSEL}}$ of delay buffer. The symbol of closed circle denotes the simulation results and the line shows the calculated results by Eq. (9). It is seen in this figure that the resolution of the DPWM generator is proportional to time delay $T_{\text{DSEL}}$ of delay buffer. Further, it is revealed that these simulated values agree well with the calculated ones. The time delay of delay buffer in the proposed circuit is set at 0.10ns. Therefore the resolution against the output voltage of the DPWM generator is 0.054 from Eq. (9) as shown in this figure. Moreover, $K_{DA}$ becomes 0.1195 by Eq. (6). In this case, $f_s=100kHz$, $E_i=20V$, $E_o^* = 5V$, $r=0.165\Omega$, $R=5\Omega$, $R_S=0.05\Omega$, $L=188\mu H$, $C=100\mu F$, $\Delta c_c=200$. $E_c=11V$, $V_{thc}=1.71V$, $\tau_c=50\mu sec$. So, the ratio of resolution of the DPWM generator is 0.27% against the output voltage.

V. CONCLUSION

The dynamic characteristic of proposed novel digital peak current-injected control dc-dc converter is discussed.

As a result, it is clarified that the transient time is suppressed to within 151μsec and this result is approximately 85% smaller than the conventional digital control dc-dc converter. The undershoot of output voltage is suppressed to within 2.8% and this result is approximately 53%, the overshoot of reactor current is suppressed to within 18% and this result is approximately 57% small than that of the conventional control method. Furthermore, the ratio of resolution of the DPWM generator against the output voltage is 0.27% and is satisfied to apply the commercial power supply unit.

We confirm that these results are useful to realize the next generation model of the switching power supply.

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