Control Method for Autonomous Changing the Number of DC-DC Converters to Improve Efficiency

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Abstract — In this paper, a control method for autonomous changing the number of parallel driven DC-DC converter is proposed. In order to improve efficiency of the parallel driving, the number of parallel driven converters is dynamically changed for the variations of the load current. The changing point of the load current is determined as a function by the number of parallel driven converters and the parameters of the converter. The calculated changing points are usable in practical use with the experimental power loss of the converters.

I. INTRODUCTION

The load current range of the power supplies becomes higher and wider, and the importance of the power supply system increases. The parallel driving including multi-phase driving are useful to realize high efficiency at heavy load, and also to secure redundancy of the power supply system.

The DC-DC converter modules become very thinner and smaller recently.[1] Applance of those small converter modules to the parallel driving is expected to realize small size and simple designing of the high efficiency power supply.

However, the parallel driving generally decreases the efficiency at light load as the number of parallel driving increases because of its each fixed loss which does not related to the load current. Therefore, dynamically changing the number of parallel driving is suggested to optimize efficiency for the variations of the load. [2][3]

In order to optimize efficiency by changing the number of parallel driving, it is necessary to find the threshold load current. In this paper, we propose the method to determine the threshold load current simply from the number of parallel driving and the parameters of the converter.

II. THEORETICAL CONTROL METHOD

A. The concept of parallel driving the converters

Fig.1 and Fig.2 show an example of parallel driven buck type DC-DC converter circuit and its efficiency, respectively. \( n \) is the number of the parallel driven converters. Input lines and output lines are connected to each other. The parallel driven converters are assumed to have the same performance.

From Fig.2, when the output load current increases, the efficiency generally increases at light load area, and decreases at heavy load area.

In order to realize higher efficiency at heavy load, the parallel driving will be quite useful.

B. The elements of the power loss

First of all, in order to find the intersection of the efficiency curve by calculation, confirming the function which represents the efficiency curve of each buck converter is required.

The power loss of each buck converter in Fig.1 is approximately divided to the following elements.[4]

\[
P_{\text{DC loss}} = R_{\text{dc}} \cdot i_{\text{in}}^2
\]

\( R_{\text{dc}} \): DC resistance of the inductor
\( i_{\text{in}} \): Output load current of single DC-DC converter

If the number of the parallel driven converters is changed at the intersection of the efficiency curve of increased or decreased the number of converters, total efficiency can keeps highest at all times.

Therefore, this paper proposes the method to calculate the intersection of the efficiency curves in the following sections.
AC loss of the inductor ($P_{\text{Lac}}$);

\[
P_{\text{Lac}} = R_{\text{Lac}} \cdot I_{\text{Lac}}^2 = R_{\text{Lac}} \cdot \left( \frac{1}{2\sqrt{3}} \Delta I_L \right)^2
\]

\[
= \frac{R_{\text{Lac}}}{12} \cdot \left( V_i - V_o \cdot \frac{1}{L} \cdot f \cdot I_{\text{Lac}} + \frac{1}{f} \right)^2
\]

\[
R_{\text{Lac}}: \text{AC resistance of the inductor}
\]

\[
I_{\text{Lac}}: \text{AC current of the inductor}
\]

\[
\Delta I_L: \text{Ripple current of the inductor}
\]

\[
V_i: \text{Supply voltage}
\]

\[
V_o: \text{Output voltage of the DC-DC converter}
\]

\[
L: \text{Inductance}
\]

\[
f: \text{Switching frequency}
\]

Gate charge loss of switching MOSFETs ($P_{\text{Qg}}$);

\[
P_{\text{Qg}} = (Q_{\text{gH}} \cdot V_{\text{gH}} + Q_{\text{gL}} \cdot V_{\text{gL}}) \cdot f
\]

\[
Q_{\text{gH}}: \text{Gate charge of high side MOSFET}
\]

\[
Q_{\text{gL}}: \text{Gate charge of low side MOSFET}
\]

\[
V_{\text{gH}}: \text{Gate drive voltage of high side MOSFET}
\]

\[
V_{\text{gL}}: \text{Gate drive voltage of low side MOSFET}
\]

Loss of the junction capacitance of the MOSFETs ($P_{\text{QDS}}$);

\[
P_{\text{QDS}} = \frac{1}{2} (C_{\text{DSH}} + C_{\text{DSD}}) \cdot V_i^2 \cdot f
\]

\[
C_{\text{DSH}}: \text{Junction capacitance of high side MOSFET}
\]

\[
C_{\text{DSD}}: \text{Junction capacitance of low side MOSFET}
\]

Conduction loss of the high side MOSFET ($P_{\text{ONH}}$);

\[
P_{\text{ONH}} = \frac{V_i}{V_o} \cdot R_{\text{ONH}} \cdot \left( \frac{I_{\text{peak}}^2 + I_{\text{bottom}}^2 + I_{\text{peak}} \cdot I_{\text{bottom}}}{3} \right)
\]

\[
= \frac{V_i}{V_o} \cdot R_{\text{ONH}} \cdot \left( \frac{I_m^2 + \frac{\Delta I_L^2}{12}}{3} \right)
\]

\[
R_{\text{ONH}}: \text{On resistance of high side MOSFET}
\]

\[
I_{\text{peak}}: \text{Peak current of the inductor}
\]

\[
I_{\text{bottom}}: \text{Bottom current of the inductor}
\]

\[
I_m: \text{Supply current of control IC}
\]

\[
V_{\text{CC}}: \text{Supply voltage}
\]

\[
IV: \text{Output voltage of the DC-DC converter}
\]

\[
L: \text{Inductance}
\]

\[
f: \text{Switching frequency}
\]

Conduction loss of the low side body diode ($P_{\text{BDI}}$);

\[
P_{\text{BDI}} = t_d \cdot f \cdot \left( I_{\text{peak}} \cdot I_{\text{bottom}} + V_o \cdot I_{\text{bottom}} \right)
\]

\[
= 2t_d \cdot f \cdot V_o \cdot I_m \quad (11)
\]

\[
V_o: \text{Body diode voltage of low side MOSFET}
\]

Turn-on and Turn-off loss of the high side MOSFET ($P_{\text{SW}}$);

\[
P_{\text{SW}} = \frac{1}{2} \cdot \frac{V_i}{V_o} \cdot f \cdot \left( I_{\text{peak}} + I_{\text{bottom}} \right) \cdot \left( t_r + t_f \right)
\]

\[
= \frac{1}{2} \cdot \frac{V_i}{V_o} \cdot f \cdot \left( I_{\text{peak}} + I_{\text{bottom}} \right) \cdot \left( t_r + \frac{t_f - t_r}{2} \right) \cdot \Delta I_L
\]

\[
t_r: \text{Rise time at switching on of high side MOSFET}
\]

\[
t_f: \text{Fall time at switching off of high side MOSFET}
\]

Power consumption of the control IC ($P_{\text{CTRL}}$);

\[
P_{\text{CTRL}} = V_i \cdot I_{\text{CC}}\quad (13)
\]

\[
I_{\text{CC}}: \text{Supply current of control IC}
\]

The total power loss of each buck converter $P_L$ is calculated by the addition of the power loss elements above.

When supply voltage $V_i$, output voltage $V_o$ and switching frequency $f$ are fixed, the power loss $P_{\text{Lac}}$ of (1), $P_{\text{ONH}}$ of (7) and $P_{\text{ONL}}$ of (8) are the quadratic functions of $I_m$, the power loss $P_{\text{BDI}}$ of (11) and $P_{\text{SW}}$ of (12) are the linear functions of $I_m$, and other power losses are constant value.

Therefore, total power loss $P_L$ is represented approximately by the quadratic function of load current $I_m$.

\[
P_L = (P_{\text{Lac}} + P_{\text{ONH}} + P_{\text{ONL}} + P_{\text{BDI}} + P_{\text{SW}})
\]

\[
+ P_{\text{Lac}} + P_{\text{Qg}} + P_{\text{QDS}} + P_{\text{CTRL}}\quad (14)
\]

\[
= aI_m^2 + bI_m + c
\]

Furthermore, total power loss $P_L$ can also be approximated to the quadratic functions of $I_m$ by the numerical analysis such as the polynomial regression from the real experimental data of the operated buck converter.

C. The calculation of the intersection on efficiency curve

The power loss of the single converter $P_L$ is approximates to a quadratic function of the load current $I_m$ as follows:

\[
P_L(i_m) = aI_m^2 + bI_m + c\quad (16)
\]

When the number of the parallel driven converters is $n$, the total load current $i_o$ and the efficiency $\eta_n(i_o)$ of parallel driven converters are shown as (17) and (18) respectively.

\[
i_o = n \cdot I_m\quad (17)
\]

\[
\eta_n(i_o) = \frac{V_o i_o}{V_o i_o + n \cdot P_L(i_m)} = \frac{V_o i_o}{\frac{a}{n} I_m^2 + (b + v_o) I_m + c
\]

When the number of the parallel driven converters increase to $n+1$, the total load current $i_o$ and the efficiency $\eta_{n+1}(i_o)$ of parallel driven converters are shown as (19) and (20) respectively.
\[ i_n = (n+1) \cdot i_m \quad (19) \]
\[ \eta_{n+1}(i_m) = \frac{v_s j_s + (n+1) \cdot p_2(i_m)}{v_s i_s + (n+1) \cdot p_2(i_m)} = \frac{a}{n+1} i_n^2 + (b + v_o) i_n + c(n+1) \quad (20) \]

From Fig.2, the ideal changing point is the intersection of the efficiency curves (18) and (20). Therefore, the intersection load current \( i_{n+1} = I_{th,n} \) of the efficiency curve is calculated from the functions (18) and (20) as follows.

\[ \eta_n(I_{th,n}) = \eta_{n+1}(I_{th,n}) \quad (21) \]
\[ \frac{a}{n} I_{th,n}^2 + (b + v_o) I_{th,n} + c(n+1) = \frac{a}{n+1} I_{th,n}^2 + (b + v_o) I_{th,n} + c(n+1) \quad (22) \]

\[ I_{th,n} = \sqrt{\frac{c}{a}} n(n+1) \quad (23) \]

Therefore the intersection load current of each converter \( I_{th,n} \) is calculated as follows;

\[ I_{th,n} = \frac{I_{th,n}}{n} = \sqrt{\frac{c}{a}} \frac{n+1}{n} \quad (24) \]

Equation (24) means that the intersection load current of each converter is determined by the coefficient of the quadratic function \( a \) and \( c \) which represents the efficiency curve as (16), and the number of parallel driven converters \( n \).

Furthermore, since the coefficient \( a \) and \( c \) are fixed value, the intersection load currents of (23) and (24) is only the function of \( n \).

D. Detection circuit

From (24), the intersections of the efficiency curves are calculated by comparing the sensed load current \( i_m \) with the reference voltage which related to \( n \).

Therefore, the detection circuit of the efficiency curve intersection can be composed with the comparator which compares the sensed load current \( i_m \) and the reference voltage \( V_{REF} \) as shown in Fig.3.

In Fig.3, the coefficient “\( \alpha \)” is multiplied to both of the sensed current “\( i_m^2 \)” and the reference voltage “\( c/a (n+1)/n \)” in order to operate the comparator in its common-mode range.

E. Verification of the proposed method

In order to verify the proposed method to find the intersection of the efficiency curves, we compared the power loss curves and the efficiency curves with the experimental result, theoretical quadratic function by the equations from (1) to (15), and approximated quadratic function by the polynomial regression of the experimental result.

The experimental power loss and the efficiency are evaluated by using trial products of 3A built-in MOSFET synchronous buck converter IC which is shown as Fig.5.

The circuit design parameters of the converter parts and ICs are shown in Table.1. Therefore, equations from (1) to (15) can be calculated by the parameters in Table.1.
The power loss $P_L$ is calculated from (14) and the Table.1 as follows;

$$P_L(i_m) = 0.214i_m^2 + 0.0745i_m + 0.122 \quad (25)$$

The experimental power loss of the buck converter is shown in Fig.6. It also shows the theoretical power loss which is calculated from the function of (25). The theoretical power loss curve is almost as same as the experimental power loss curve. Therefore the theoretical function (25) has few errors at modeling is confirmed.

The experimental power loss curve in Fig.6 can be approximated by using polynomial regression. The approximated power loss function is shown as follows;

$$P_L(i_m) = 0.234i_m^2 + 0.0311i_m + 0.126 \quad (26)$$

Therefore, the each coefficient $a$, $b$ and $c$ of quadratic function (16) are shown in Table.2.

<table>
<thead>
<tr>
<th></th>
<th>$a$</th>
<th>$b$</th>
<th>$c$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Theoretical function</td>
<td>0.214</td>
<td>0.0745</td>
<td>0.122</td>
</tr>
<tr>
<td>Approximated function</td>
<td>0.234</td>
<td>0.0311</td>
<td>0.126</td>
</tr>
</tbody>
</table>

The efficiency curves are shown in Fig.8. It compares with the experimental result, theoretical function of (25), and approximated function of (26).

It is realized the theoretical curve and the approximated curve include some errors from the comparison to the experimental result.

The intersections of efficiency curves which are calculated as (23), (24) and Fig.3 are shown in Table.3.

<table>
<thead>
<tr>
<th></th>
<th>Theoretical</th>
<th>Approximated</th>
</tr>
</thead>
<tbody>
<tr>
<td>$c/a$</td>
<td>$\alpha$</td>
<td>$c/a$</td>
</tr>
<tr>
<td>1</td>
<td>1.140</td>
<td>1.068</td>
</tr>
<tr>
<td>2</td>
<td>0.855</td>
<td>1.849</td>
</tr>
<tr>
<td>3</td>
<td>0.760</td>
<td>2.615</td>
</tr>
<tr>
<td>4</td>
<td>0.713</td>
<td>3.376</td>
</tr>
</tbody>
</table>

Fig.7 shows the experimental efficiency curves with the calculated intersections which are shown in Table.3. The calculated intersections are almost as same as the intersection of the experimental curves.

Each difference between the intersections of the experimental curves and the calculated intersections are shown in Table.4.

<table>
<thead>
<tr>
<th></th>
<th>Theoretical</th>
<th>Approximated</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Delta I_{th,n}$</td>
<td>$\Delta \eta_n(I_{th,n})$</td>
<td>$\Delta I_{th,n}$</td>
</tr>
<tr>
<td>1</td>
<td>2.84%</td>
<td>-0.14%</td>
</tr>
<tr>
<td>2</td>
<td>3.09%</td>
<td>-0.08%</td>
</tr>
<tr>
<td>3</td>
<td>2.59%</td>
<td>-0.05%</td>
</tr>
<tr>
<td>4</td>
<td>2.43%</td>
<td>-0.04%</td>
</tr>
</tbody>
</table>
III. CONCLUSION

We proposed the new method to change the number of parallel driven buck type DC-DC converters to improve efficiency. If you can represent the power loss of the converter to the quadratic function, the threshold load current of changing the number of converters can be represented simply from the number of parallel driven converters and the parameters of the converter.

We used the buck converter to explain the method in this paper. However this method is usable not only buck converters, but also any converters which the power loss of the converter can be represented to the quadratic function.

We will examine to apply this method with variable input and output voltage, frequency and temperature in near future.

REFERENCES


