1MHz Switching Frequency POL
with a Fast Response Digital Controller

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Abstract—In this paper, the proposed hardware logic type
digital controller for on-board SMPS which has a very small
time-delay in control loop has been described. Some
experimental has been done including evaluation of load current
change and frequency characteristic of open loop transfer
function. These results have been revealed that the proposed
circuit could be suppressed the time delay to sub–micro second
order.

I. INTRODUCTION

Digital electronic products have been spreading quickly by
the advancement of the integrations technologies. ICs, DSPs
and FPGAs require a high performance and a high speed due
to the trend. Along with the situations, the power consumption
is increasing. To suppress the power consumption, the power
supply voltage is getting lower toward to sub 1V. Because of
the severe voltage margin by the lower power supply voltages,
special SMPS, point of load (POL) is disposed very near to the
load. The requirements of the control circuit of POL are
becoming adaptive, more accurate, higher speed and lower
cost.

For the control purpose, pulse width modulation (PWM)
control is a one of appropriate technique. Digital control or
digital pulse width modulation (DPWM) can accomplish
robust and flexible power control with soft-tuned parameters
and will become popular control technique [1-21]. Therefore,
term of development is shorter than analog controller.
Although, there are some disadvantages in cost of production
and speed, against analog control circuit. We had proposed
hardware-logic based digital PWM control circuit is effective
to such requirements [22-26]. In this paper, the proposed DPWM
control method’s principles of operation and circuit
configurations are described firstly. At the next, the proposed
technique is confirmed with some experiments.

II. THE CIRCUIT CONFIGURATION OF GENERAL DPWM
CONTROLLER FOR POL

The circuit configuration of general DPWM controlled
POL is shown in Fig. 1(a). This topology has two major
time-delay problems.

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technique is confirmed with some experiments.

A. The circuit configuration of the proposed DPWM-POL

Figure 2 shows the main and the control circuit
configuration of the proposed DPWM-POL in this research.

First, time-delay occurs at A/D converter with the conversion-
delay. And, the calculation time of digital controller is another
problem. Both of the time-delay directly effects on the
response speed of the control circuit and influences stability of
the control. Total of the delay time will be described as the
discrete time-delay factor $V_q/Z$ in the control loop shown in
Fig.1(b) where $V_q$ is a coefficient constant.

III. THE PROPOSED DPWM CONTROLLER FOR POL

The circuit configuration of general DPWM controlled
POL is shown in Fig. 1(a). This topology has two major
time-delay problems.
Digital Controller

Main POL circuit is a quite ordinary non-isolated buck converter. The control circuit is composed with D/A converter, analog comparator, digital controller and drive circuit.

The analog timing converter (ATC) block shown in Fig. 2 (a) is composed with D/A converter and analog comparator. In Fig. 2(b), the control block diagrams are shown. ATC block, PID control calculation block and up-counter block for gate pulse creation, are all in parallel and synchronized with the system clock $f_{CLK}$.

B. The control circuit configuration of the proposed DPWM-POL

Figure 3 shows the precise control circuit configuration, and Fig. 4 shows control signal flow of the proposed DPWM-POL. Let’s take a look at the signal flow.

As mentioned above, all blocks are synchronized with the system clock $f_{CLK}$. Memory 1 is used the look-up table method, and can store waveform values not only triangle or saw tooth but any waveforms. In this paper, the step-down saw tooth wave form is employed. $V_{ref}$ is the maximum output voltage of DAC. The output voltage $E_o$ of POL is compared with the output voltage of D/A converter in the ATC block, successively. The comparator’s output is read out to the latch signal to each D-ff at the timing that of $E_o$ was sensed. Also, the look-up table method is used for the duty ratio calculation with memory 2, 3 and 4. Especially, the duty ratio data which is pre-calculated with the value of $E_o$, are stored in memory 2.

The duty ratio data is read out from memory2 according to $f_{CLK}$. At the timing of $E_o$ sensed, one of the duty ratio data is chosen and transferred to $u(k)$ in D-FF4, where $k$ is the number of switching term.

![Figure 2. Circuit configuration of proposed DPWM-POL](image1)

![Figure 3. The system configuration of proposed control circuit](image2)

![Figure 4. Control signal flow](image3)
At the digital comparator, \( u(k) \) is compared with up-counter data, and converted to real-time analog PWM waveforms. On-term \( T_{on}(k) \) of DPWM signal of switching term \( k \) is decided by \( u(k) \). In parallel with the processing of ATC block, the \( u(k) \) is called with system clock and latched by ATC output as trigger. At the last of the switching term, \( u(k) \) is preset maximum value by PR signal generator for preparing next term.

The delay of the proposed control circuit is mostly dominated with the calling and the loading time of memory 2.

Because of the small delay of this control technique, the sensed \( E_O \) data can reflect on-term of the same switching term.

C. PID control with Look-up Table

\( u(k) \) which is stored in memory 2 is pre-calculated by general PID digital control laws as

\[
u(k) = u_{ref} + K_P e(k) + K_I n_I(k) + K_D (e(k) - e(k-1)) \tag{1}
\]

where \( u_{ref} \) is a reference value of \( u(k) \), \( e(k) \) is an digitalized error value between \( r \) which is digitalized reference voltage \( V_{ref} \) and, \( y_1(k) \) is output data of up-counter in switching term \( k \) as

\[
e(k) = y_1(k) - r \tag{2}
\]

\( K_P, K_I \) and \( K_D \) are a proportional gain, an integral gain and a derivative gain, respectively, \( n_I(k) \) is integral factor, that is

\[
n_I(k) = n_I(k-1) + e(k) \tag{3}
\]

At the timing of the latch signal is becoming high, \( y_1(k-1) \) is latched to \( y_2(k-1) \) as

\[
y_2(k-1) = y_1(k-1) \tag{4}
\]

From above equations, Eq.(1) can be transformed to

\[
u(k) = u_{ref} - (K_P + K_I)r + A[y_1(k) + \frac{K_I}{A}n_I(k-1) - \frac{K_P}{A}y_2(k-1)] \tag{5}
\]

where

\[
A = K_P + K_I + K_D \tag{6}
\]

\[
a = \frac{K_I}{A}n_I(k-1) \tag{7}
\]

\[
b = \frac{K_P}{A}y_2(k-1) \tag{8}
\]

Memory 3 and memory 4 store \( a \) and \( b \), respectively.

In (5), \( a - b \) in the term \( k \) is pre-calculated in the term \( k-1 \) and the obtained value becomes the initial value of programmable counter of the term \( k \). And, \( address' \) which indicates address of memory 2 is incremented with system clock and \( u(k) \) is called from memory 2, simultaneously.

\[
address' = y_1(k) + a - b \tag{9}
\]

From (5) and (9),

\[
u(k) = u_{ref} - (K_P + K_I)r + A[address'] \tag{10}
\]

Therefore, \( u(k) \) is determined as soon as \( E_O \) is sensed.

Table I shows the address and data of memory2 at \( K_P = 5, K_I = 0 \), \( u_{ref} = 86 \), \( r = 40 \) in (10). Figure 5 shows address and duty ratio at Table I.

You can see, Table I data have linear and nonlinear domain. And, if \( K_P \) becomes more higher, linear domain becomes shorter.

D. Overvoltage protection logic circuit

If trigger does not occur, proposed circuit outputs overvoltage. Therefore, we use overvoltage protection logic circuit. Figure 6 shows overvoltage protection circuit for proposed circuit. It is composed with selector, D-ff, sample pulse generator and reset pulse generator for D-ff.

\[
<table>
<thead>
<tr>
<th>\text{Address}</th>
<th>\text{Data}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>22</td>
<td>0</td>
</tr>
<tr>
<td>23</td>
<td>1</td>
</tr>
<tr>
<td>24</td>
<td>6</td>
</tr>
<tr>
<td>25</td>
<td>11</td>
</tr>
<tr>
<td>26</td>
<td>16</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>119</td>
<td>481</td>
</tr>
<tr>
<td>120</td>
<td>486</td>
</tr>
<tr>
<td>121</td>
<td>491</td>
</tr>
<tr>
<td>122</td>
<td>496</td>
</tr>
<tr>
<td>123</td>
<td>500</td>
</tr>
<tr>
<td>511</td>
<td>500</td>
</tr>
</tbody>
</table>

![Figure 5. Address vs. duty ratio at Table I](image-url)

Table I. Address and data of memory2 at \( K_P = 5, K_I = 0 \)
IV. EXPERIMENTAL RESULTS

A. Specifications

The proposed control system with prototype circuit is shown in Fig. 8. The digital controller part is designed with FPGA module DE0-Nano with Altera Cyclone IV. The total number of logic elements is 163 including all of the memory sections. All memory blocks, memory 1, memory 2, memory 3 and memory 4, are including in the logic elements. Texas Instruments DAC900 is used as DAC. Linear Technology LT1719 is used as analog comparator. Fairchild FDMF6705V is used as MOSFET and driver. The DC-DC converter topology is basically same as buck converter in Fig.2. The experimental conditions are shown in Table III. Figure 9 shows static state waveforms.

B. Experimental set-up

Some experiments are performed to verify the proposed controller.

1) Static characteristic and load current change transient response

Figure 10 shows experimental set-up of static characteristic and load current change dynamic response. We measured output voltage $E_0$, $V_{comp}$, PWM signal and output current $I_o$ with analog probe, $V_{comp}$ and $u(k)$ in Fig. 3 with digital probe. Current change slew rate is 50A/µs.

2) Open loop transfer function

Figure 11 shows experimental set-up of open loop transfer function. We used FRA50976 at measurement. FRA50976 is frequency response analyzer from NF Corporation.

![Figure 8. Prototype circuit](image)
### TABLE III. EXPERIMENTAL CONDITIONS

<table>
<thead>
<tr>
<th>Parameters / Components</th>
<th>Value / name</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage ( E_i )</td>
<td>12V</td>
</tr>
<tr>
<td>Output target voltage</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output current ( I_o )</td>
<td>0.3A ~ 0.9A</td>
</tr>
<tr>
<td>Switching frequency ( f_s )</td>
<td>1MHz</td>
</tr>
<tr>
<td>Choke inductor ( L )</td>
<td>3.3 ( \mu )H</td>
</tr>
<tr>
<td>Output capacitor ( C_o )</td>
<td>10( \mu )F</td>
</tr>
<tr>
<td>Proportional gain ( K_p )</td>
<td>5, 10</td>
</tr>
<tr>
<td>Integral gain ( K_i )</td>
<td>0</td>
</tr>
<tr>
<td>Differential gain ( K_d )</td>
<td>0</td>
</tr>
<tr>
<td>( V_{\text{ref}} )</td>
<td>1.6</td>
</tr>
<tr>
<td>( f_{CL} )</td>
<td>500MHz</td>
</tr>
<tr>
<td>Current change slew rate</td>
<td>50A/\mu s</td>
</tr>
<tr>
<td>Digital PWM resolution</td>
<td>9bit</td>
</tr>
<tr>
<td>Dr. MOS (MOSFET and driver)</td>
<td>Fairchild FDMF6705V</td>
</tr>
<tr>
<td>Analog comparator</td>
<td>Linear Technology LT1719</td>
</tr>
<tr>
<td>D/A converter</td>
<td>Texas Instruments DAC900</td>
</tr>
<tr>
<td>FPGA</td>
<td>Terasic DE0-Nano (Cyclone IV)</td>
</tr>
</tbody>
</table>

\( L_c \): 1A/div (CH4), \( V_{\text{comp}}\) (digital):D9, u(k):D0-D8, respectively. Bottom figure is an enlargement of a part of top figure and it shows reflection time.

**C. Measurement Results**

1) **Static characteristics**

Figure 12 shows static characteristic at \( K_p=10 \). It shows when load current is 0.3~0.9, output voltage is \( \pm 3\% \) of target voltage.

2) **Load current change transient response**

Figure 13 and 14 show experimental waveforms of load current change transient response. All figures show \( E_o\): 100mV/div(CH1), PWM: 3V/div(CH2), \( V_{\text{comp}}\): 3V/div(CH3),

![Figure 9](image)

Figure 9. Static state waveforms, \( E_o\):500mV/div(CH1), \( V_{\text{ref}}\):1V/div(CH2), \( V_{\text{comp}}\): 2V/div(CH3), PWM: 2V/div (CH4), \( V_{\text{comp}}\) (digital):D9, u(k):D0-D8

![Figure 10](image)

Figure 10. Experimental set-up ststic characteristic and load current change transient response

![Figure 11](image)

Figure 11. Experimental set-up open loop transfer function

![Figure 12](image)

Figure 12. Static characteristic of converter at \( K_p=10 \)
Undershoot = 160mV
Recovery time = 10.4μs

Figure 13. Load change from 0.3 to 0.9A (KP=10)

Recovery time = 10.9ns
Reflection time = 10.9ns

Figure 14. Load change from 0.9 to 0.3A (KP=10)

TABLE IV COMPARISON WITH PRIOR WORKS.

<table>
<thead>
<tr>
<th>[18]</th>
<th>[19]</th>
<th>[20]</th>
<th>[21]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>4.7μH</td>
<td>2.2μH</td>
<td>4.7μH</td>
<td>4.7μH</td>
</tr>
<tr>
<td>C</td>
<td>4.7μF</td>
<td>11μF</td>
<td>22μF</td>
<td>22μF</td>
</tr>
<tr>
<td>Converter type</td>
<td>buck</td>
<td>buck</td>
<td>buck</td>
<td>buck</td>
</tr>
<tr>
<td>f</td>
<td>1M Hz</td>
<td>1M Hz</td>
<td>782kHz</td>
<td>4M Hz</td>
</tr>
<tr>
<td>Load current step</td>
<td>0.6A</td>
<td>0.275A</td>
<td>0.59A</td>
<td>0.16A</td>
</tr>
<tr>
<td>Input voltage</td>
<td>3V</td>
<td>5V</td>
<td>2.7-4.2V</td>
<td>3.3V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>1.8V</td>
<td>1.6-3.2V</td>
<td>0.9-1.2V</td>
<td>1.5V</td>
</tr>
<tr>
<td>Settling time</td>
<td>∼20μs</td>
<td>2μs</td>
<td>84.5μs</td>
<td>15μs</td>
</tr>
</tbody>
</table>

Figure 13 and 14 show 0.3–0.9A load transient response at KP=10. Figure 13 shows light to heavy load transient response and output voltage settled in 10.4μs, under shoot is 160mV. Figure 14 shows heavy to light load transient response and output voltage settled in 3.2μs, over shoot is 58mV.

From these figures, the reflection time from $V_{\text{comp}}$ to $u(k)$ change is 11.0ns even in the worst case. Table IV is comparing the settling time of the output voltage from the proposed digitally controlled switching converter with prior work. It shows that the proposed digital controller achieves much faster output settling time than existing digital compensators [18]–[21].

3) Open loop transfer function

Figure 15 is the result of frequency characteristics of open loop transfer function when $K_P=5$, $K_I=0$. Colored line with $I_o=0.3$ and gray line one with $I_o=0.7$.

Figure 16 is the result of frequency characteristics of open loop transfer function when $K_P=10$, $K_I=0$. Colored line with $I_o=0.3$ and gray line one with $I_o=0.7$. From Fig.15 and 16, it can be seen that phase margin is about 49 degree and gain margin is about 20 dB in worst case. From the results, the time-delay of proposed circuit has small effects to the control loop.
V. CONCLUSIONS AND FUTURE WORK

In this paper, the hardware logic type digital controller for on-board SMPS, which has a very small time-delay in control loop, is confirmed with some experiments including frequency characteristic. As the future work, analysis of the proposed control system.

REFERENCES


APPENDIX

To reveal the merit of the use of the DAC and comparator in spite of the ADC for sensing output voltage $E_o$, we have made survey at the view point of the market price and the conversion rate. Figure 17 shows the results of comparison of several parallel interface DACs and ADCs. The horizontal axis represents the market price for 50 pcs, and the vertical axis represents the conversion rate. The products from four major companies A, B, C, and D, are compared. ADCs are shown in square mark, and DACs are triangle mark. Apparently, almost all of DACs are relatively cheaper than ADC in every grade conversion rate.

From the above, it is apparent that the proposed analog voltage sensing part which is composed with DAC and analog comparator is superior to conventional sensing technique with ADC in the point of view of high speed response and cost.

![Figure 17. Comparing 12bit ADCs and 12bit DACs](image)